IN THE SPECIFICATION:

Please amend the Specification as follows, with underlining denoting replacements/additions and strikethrough denoting deletions.

At page 11, lines 14-20, please amend the paragraph as follows:

"The thyristor body 210 is coupled in series with the pass device 260 at the N+ emitter region 218, which is shared with the pass device 260 as a first source/drain region. The pass device further includes a second source/drain region 264, separated from the N+ emitter region 218 by a P-well region 266. A gate 268 is separated from the P-well region 266 by a dielectric material 267, with insulative sidewall spacers 265 and 263 on opposing sides of the gate ~~368~~ 268 and with a salicide region 269 on the gate 268 for making electrical contact thereto.

At page 14, lines 1-12, please amend the paragraph as follows:

"FIG. 4 is another thyristor-based semiconductor device 400, similar to the device 200 shown in FIG. 2, but formed using a third word line 490, which has been subsequently removed, as a mask during implant of an N-base region 414, according to another example embodiment of the present invention. Essentially, the third word line 490 is formed over a lightly-doped portion ~~211~~ 411 of an emitter region ~~212~~ 412 with sidewall spacers 491 and 492 on opposing sidewalls thereof. The combination of the third word line 490 and sidewall spacers 491 and 492 are used as a mask during an N-base implant to form N-base region 414 (as well as a mirrored N-base region adjacent to sidewall spacer 491). After the N-base implant, the third word line is removed (*e.g.*, via etching) and a P+ implant is used to form a

P+ doped emitter portion 430. A salicide material 413 is formed on the P+ doped emitter portion 430, wherein electrical contact is made to the portion 271 of the first metal layer via Vref line 270."

At page 15, lines 1-9, please amend the paragraph as follows:

"FIG. 5B shows a thyristor-based semiconductor device 501, similar to the device 500 shown in FIG. 5A, and without the third word line 490, according to another example embodiment of the present invention. In this example embodiment, the P+ anode 530 implant is effected using a mask to prevent the lightly-doped region 411 from being implanted. Spacer/insulating material 522 and 523 is formed over the device ~~510~~ 501 after the P+ doped emitter portion 530 is formed, or, in one implementation, before the P+ doped emitter portion 530 is formed, wherein the spacer/insulating material 522 and 523 is used as a mask. A region 533 over the P+ doped emitter portion 530 is salicided, to which contact is made via contact 270 as discussed above."